Docket No.: 32172-188433
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Magill et al.	Art Unit: 2619
Application No: 10/606,753	Examiner: B. O'connor
Confirmation No: 5555	
Filed: June 27, 2003	Atty. Docket No: 32172-188433
For: SCHEDULING PACKETS FOR SWITCH MEMORY (PB 02 0011)	Customer No: 26694 PATENT TRADEMARK OFFICE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Final Office Action dated July 10, 2008 (hereinafter 'the Office Action'), Appellant respectfully submits this Pre-Appeal Brief Request for Review pursuant to the "New Pre-Appeal Brief Conference Pilot Program" (1296 Off. Gaz. Pat. Office 67 (July 12, 2005)) and the "Extension of the Pilot Pre-Appeal Brief Conference Program" (1303 Off. Gaz. Pat. Office 21 (February 7, 2006)). Appellant also submits herewith a Notice of Appeal pursuant 37 C.F.R. § 41.31(a)(1), the claims having been finally rejected.

I. INTRODUCTORY REMARKS

Claims 1-19 are pending in the application and stand finally rejected. The Appellant believes, however, that the rejections set forth in the Office Action are clearly improper based upon error(s) in fact and the failure to establish a prima facie case of obviousness. In view of the following remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, the Appellants respectfully traverse the rejection and request careful reconsideration by the pre-appeal brief review panel.

II. CLAIM REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 1-3, 8-9, 12, and 17-19 stand rejected under 35 U.S.C. §103(a) as being obvious over by H. Jonathan Chao and Li-Shen Chen, *Delay-Bound Guarantee in Combined Input-Output Buffered Switches*, GLOBAL TELECOMMUNICATIONS CONFERENCE, 2000. GLOBECOM '00. IEEE, November 27, 2000 – December 1, 2000, Vol. 1, pgs. 515-524 (hereinafter Chao) in view of U.S. Patent No. 7, 177,314 to Wu et al. (hereinafter 'Wu'). In finally rejecting the claims, the Examiner made several factual mistakes and applied improper legal standards in an attempt to establish a prima facie case of obviousness. Applying proper standards, Chao in view of Wu does not support a prima facie rejection, and the evidence is sufficient to rebut a prima facie case of obviousness.

The rejection is therefore respectfully traversed for at least the reasons presented in the Remarks Section (pages 6-11) of Applicants' Response filed March 27, 2008 and the Remarks Section (pages 7-12) of Applicants' Response filed June 20, 2007, which are hereby incorporated by reference.

Regarding claim 1, Chao and Wu, taken either singly or in any reasonable combination, do not disclose or suggest the claimed invention for at least the following two reasons.

First, Chao does not disclose or suggest "switch fabric having memory," as recited in claim 1. On pages 2-3 and 13, the Office Action appears to argue that Chao inherently discloses a switch fabric having memory. Applicants have clearly rebutted the Office Action's assertions by (1) showing that the Office Action made several factual errors while interpreting Chao and (2), based on a correct understanding of Chao, Chao neither explicitly or inherently discloses a switch fabric having memory.

As Applicants discussed in their previous responses noted above, Chao discloses the implementation of an HLS scheme on a non-blocking switch with buffers placed at the input and output to coordinate the transition of cells across the non-blocking switch. Chao, pg. 515. **Chao defines a non-blocking switch as being internally non-blocking**. *Id.* In addition, Figure 3 of Chao does not disclose a switch fabric as the Office Action alleges. Instead, Figure 3 depicts the communication between the **Input** Port Controller (IPC), the **Output** Arbitration Processor (OAP), the **Input** Arbitration Processor (IAP), and the **Output** Port Controller (OPC) before, during, and

after a cell is transmitted through the non-blocking switch of Figure 1. Chao, pgs. 516-521. Therefore, **Figure 3 of Chao does not represent a switch fabric** as the Office Action asserts.

Furthermore, Chao does not disclose the design of the switch fabric of Figure 1 nor how cells moves through the switch fabric. Chao merely states that "a cell is transmitted across the switch" to an output buffer. Chao, pgs. 516, 517, and 521. Thus, Chao does not disclose a need for the non-blocking switch to store the packet as the packet is being transmitted through the switch. Furthermore, the non-blocking nature of the switch gives rise to the conclusion that cells are tranmitted across the switch without stopping (i.e. without being stored). The switch of Chao is similar to a **transmission line** and **not** a **storage device**. For these two reasons, **Chao does not necessarily and logically possess "switch fabric having memory," as recited in claim 1**. In re Best, 562 F.2d 1252, 1254 (CCPA 1977); *see also* MPEP 2112.01. Chao, therefore, does not inherently teach a "switch fabric having memory," as recited in claim 1. Furthermore, as Applicants have previously argued, Wu fails to overcome the deficiencies of Chao.

Second, on page 2 the Office Action states that Chao does not disclose "a controller determining input priorities for cells moving from said input queues to said switch fabric and output priorities for cells moving from said switch fabric to said output queues." Applicant's agree.

Wu fails to overcome the failings of Chao. Instead, as Applicants have previously argued as noted above, Wu does not need to determine both priorities since the crossbar performs the simple function of "mov[ing] a certain number of bytes...from the input RAM to the output RAM [during each clock cycle]." Wu, col. 5, l. 24-27. Thus Wu merely discloses scheduling and transferring bytes from the **input** RAM to the **output** RAM in accordance with a preexisting schedule and omits a discussion of cells entering or leaving the crossbar. At most, Wu teaches one priority type for moving bytes; Wu lacks any teaching or suggestion of teaching two different priority types for moving bytes. Hence Wu does not disclose or suggest "a controller determining **input priorities for cells moving from said input queues to said switch fabric** and **output priorities for cells moving from said input switch fabric to said output queues**," as recited in claim 1.

Regarding claim 2, Chao fails to disclose, at least, a controller which "orders cells stored in said switch fabric based on times of said cells to depart," as recited in claim 2. As discussed above for claim 1, Chao fails to disclose a switch fabric having memory and, therefore, cannot store or

order cells in the switch fabric, as recited in claim 2. Furthermore, Chao discloses identifying the packet with the smallest virtual finishing time in the VOQ of the input buffer, breaks the packet into cells, and transmits the cells, unimpeded, through the switch to the output buffer where the packet is reassembled. Chao, pgs. 515-517. Since cells are transmitted through the switch unimpeded, Chao does not need to "orders cells stored in said switch fabric based on times of said cells to depart," as recited in claim 1. Chao, therefore, does not teach "orders cells stored in said switch fabric based on times of said cells to depart," as recited in
claim 1.

Regarding claim 3, Chao fails to disclose, at least, "cells of said switch fabric have respective times of said cells to depart," as recited in claim 3. As discussed above for claim 1, Chao fails to disclose a switch fabric having memory and, therefore, cannot have "cells of said switch fabric," as recited in claim 3. Furthermore, Chao discloses identifying the packet with the smallest virtual finishing time in the VOQ of the input buffer and transmitting that packet, unimpeded, through the switch to the output buffer. Chao, pgs. 515-517. Since cells are transmitted through the switch unimpeded, cells in the switch of Chao do not have "times of said cells to depart," as recited in claim 3. Therefore, Chao fails to disclose a controller which "cells of said switch fabric have respective times of said cells to depart," as recited in claim 1.

Regarding claim 8, Chao and Wu, taken either singly or in any reasonable combination, do not disclose or suggest the claimed invention for at least the following reasons.

First, neither Chao nor Wu, taken either singly or in any reasonable combination, disclose or suggest "switch fabric having memory," as similarly recited in claim 1, as discussed above.

Second, neither Chao and Wu, taken either singly or in any reasonable combination, suggest "highest priority cells in said switch fabric" and "highest priority cells available for transfer in said input queues," as recited in claim 1. The Office Action appears to assert that Chao fails to teach this recitation, and Applicants agree. However, as discussed above for claim 1, Wu teaches at most one priority type for moving bytes and fails to teach two priority types for moving bytes.

Third, neither Chao and Wu, taken either singly or in any reasonable combination, suggest "prioritizing arriving cells in said input queues based on times of said arriving cells to depart, and updating cells in said input queues available for transfer to said switch fabric," as recited in claim 1.

The Office Action appears to assert that Chao fails to teach this recitation, and Applicants agree. However, Wu fails to overcome the failings of Chao. Instead, **Wu discloses transferring bytes across the crossbar in accordance with a preexisting schedule**. Wu, col. 6, l. 7-10. Wu does not teach prioritizing the bytes for transfer and then updating the bytes for transfer. Hence, Wu does not disclose or suggest "prioritizing arriving cells in said input queues based on times of said arriving cells to depart, and updating cells in said input queues available for transfer to said switch fabric," as recited in claim 8.

Claims 4-7, 9-16, 18, and 19 depend from independent claims 1, 8, or 17 and are, therefore, allowable, at least, as being dependent upon an allowable claim.

Independent claim 17 recites subject matter that is similar to that recited in claims 1 and 8, which are allowable over Choa in view of Wu as discussed above. Therefore, claim 17 is allowable for the same reasons discussed above in connection with claims 1 and 8.

III. CONCLUSION

Claims 1-19 are pending in the application. In view of the foregoing remarks, the Appellant believes that the present application is believed to be in condition for allowance. If the Pre-Appeal Review Conference believes, for any reason, that a personal communication will expedite prosecution of this application, they are hereby invited to telephone the undersigned at the number provided. Prompt and favorable consideration on the merits is respectfully requested.

Respectfully submitted,

Dated: October 10, 2008

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